REMARKS

I. Status of Claims

Claims 1-8 are pending in this application. Claims 1 and 3 are independent.

Claims 1-8 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Fujita Yoshihiro (05-053898) in view of Kobayashi et al (USP 4,550,437).

The Applicant respectfully requests reconsideration of the rejections in view of the following remarks.

II. Pending Claims

Independent claims 1 and 3 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Fujita Yoshihiro (05-053898) (hereinafter "Fujita") in view of Kobayashi et al (USP 4,550,437) (hereinafter "Kobayashi et al.").

The Office Action alleges that Fujita discloses all of the limitations of claim 1, and claim 3 which is a method claim corresponding to claim 1, except for "filtering is performed based on a computed result by the second calculator." In order to cure these deficiencies, the Office Action cites Kobayashi for disclosing the filtering.

Specifically, the Office Action indicates that, in Fujita, a first memory cell in claims 1, 3 is equivalent to an orthogonal memory cell 11 in Fig. 1, a second memory cell in claims 1, 3 is equivalent to a row memory 13 in Fig. 1, and a third memory cell in claims 1, 3 is equivalent to a column memory 19 in Fig. 1.

In contrast, as described in claims 1, 3, the first, second, and third memories of the present application are arranged "within each of a plurality of memory units" which composes a memory unit array. More specifically, in the present application, as shown in Fig. 1, memory units 10 in one form of a matrix are arranged in a memory unit array 100. In addition, as shown in Fig. 3, "a first memory cell 1" storing pixel data, "a second memory cell 2" storing first processing data, and "a third memory cell 3" storing second processing data are arranged "within the memory unit 10."

Though the Office Action does not particularly state, it seems that the Office Action is alleging that the memory unit array in claims 1, 3 (100 in Fig. 1) is equivalent to the orthogonal

memory cell 11 in Fig. 1 of Fujita. In the present application, the first, second, and third memories are arranged within each of the memory cells composing the orthogonal memory cell 11.

In contrast to the present application, in Fujita, the row memory 13, which the Office Action states as the second memory cell, and the column memory 19, which the Office Action states as the third memory cell, are arranged at the outside of the orthogonal memory cell 11, which is equivalent to the memory unit array in claims 1, 3. That is, in Fujita, the row memory 13 equivalent to the second memory cell, and the column memory cell 19 equivalent to the third memory cell, are not arranged within the plurality of memory cells composing the orthogonal memory cell 1. In other words, this structure is different from claims 1, 3.

In addition, in Fujita, the row memory 13, equivalent to the second memory cell is arranged outside of the orthogonal memory cell 11, equivalent to the memory unit array. Therefore, complicated transferring processing is inevitable in processing data of the orthogonal memory cell 11 at a row computing element 15, which is equivalent to a first calculator in claims 1, 3. That is, a row transferring circuit 17 transfers the data of the orthogonal memory cell 11 to the row memory 13, then the data is processed at the row computing element 15, and the data stored in the row memory 13 is transferred to the orthogonal memory cell 11.

Further, in Fujita, the column memory 19, equivalent to the third memory cell, is arranged outside of the orthogonal memory cell 11, equivalent to the memory unit array. Therefore, complicated transferring processing is inevitable in processing data of the orthogonal memory cell 11 at a column computing element 21, which is equivalent to a second calculator in claims 1, 3. In other words, a column transferring circuit 23 transfers the data of the orthogonal memory cell 11 to the column memory 19, then the data is processed at the column computing element 21, and the data stored in the column memory 19 is transferred to the orthogonal memory cell 11.

In contrast, in claims 1, 3 of the present application, the second and third memories as well as the first memory, are arranged "within each of a plurality of memory units" which composes the memory unit array. Therefore, it is not necessary to perform complicated transferring processing by the row transferring circuit 17 and the column transferring circuit 23. The present application realizes a simple structure without the row transferring circuit 17 and the

column transferring circuit 23.

As has been described herein above, in Fujita, there is no disclosure of "the structure in which the first, second, and third memories are comprised 'in each of memory units.'" Likewise, in Kobayashi, there is no disclosure of "the structure in which the first, second, and third memories are comprised 'in each of memory units."

For at least these reasons, the Applicant respectfully submits that claims 1 and 3, as well as their dependent claims, are patentable over the cited references.

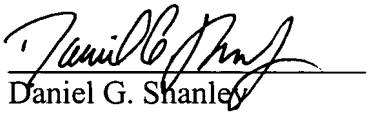
III. Conclusion

In light of the above discussion, Applicant respectfully submits that the present application is in all aspects in allowable condition, and earnestly solicits favorable reconsideration and early issuance of a Notice of Allowance.

The Office Action is invited to contact the undersigned at (202) 220-4420 to discuss any matter concerning this application. The Office is authorized to charge any fees related to this communication to Deposit Account No. 11-0600.

Respectfully submitted,

Date: August 2, 2007

By: 
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